Assignment #4

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1.

a.) 216/25 = 211 = **2048 blocks**

b.) 216 bytes of main memory => 16 bit address

256 bytes of 32 byte-per-block cache memory => 28/25 = 23 = 8 blocks of cache memory

=> **3 bits in the block field**

32 bytes per block of byte-addressable memory => 32 = 25 bytes => **5 bits in the offset field**

The remainder of bits fills the tag field => 3 + 5 = 8 => 16 – 8 => **8 bits in the tag field**

c.) \*HEX\* 43B2 => 4\*163 + 3\*162 + 11\*161 + 2\*160 = 16384 + 768 +176 + 2 = 1733010

8 blocks in cache memory => 17330 mod 8 = 2 => **it will map to the 2nd cache block**

2.

a.) Main Memory has 4K blocks with 8 words per block => (22 x 210) x 23 => 212 x 23 => 215 words in main memory and thus is has a 15 bit address. There are 4 sets in cache so => 4 = 22 => 2 bits for the set field and then that there's 3 bits for the offset field since there are 8 words per block (and it is word-addressable memory). 15 bits total - (2 set bits + 3 offset bits) = 10 bits for the tag field.

b.) First iteration of the loop: Address 8 is a miss, then the entire block is brought into Set 0. 9-15 are then hits. 16 is a miss, entire block brought into Set 1, 17-23 are hits. 24 is a miss, entire block brought into Set 2, 25-31 are hits. 32 is a miss, entire block brought into Set 3, 33-39 are then hits. 40 is a miss, entire block brought into Set 0, 41-47 are hits. 48 is a miss, entire block brought into Set 1(note we do NOT have to throw out the block with address 8 as this is 2-way set associative), 49-51 are hits. For the first iteration of the loop, we have 6 misses, and 5\*7 + 3 hits, or 38 hits. On the remaining iterations, we have 5\*8+4 hits, or 44 hits each, for 88 more hits. Therefore, we have 6 misses and 126 hits, for a hit ratio of 126/132, or 95.45%.

3.

a.) 32 M = > 25\*220 => 225 => **25 bits**

b.) 2 M => 21\*220 => 221 => **21 bits**

c.) 152410 = 00000000000000101111101002

Page size is 1024 bytes => 210 => offset is 10 bits

Virtual memory: 225/210 = 215 => page field is 15 bits

Physical memory: 221/210 = 211 => frame number field 11 bits

First 15 bits for page field => 000000000000001 => page 1 => bytes 1024 – 2047 which is in frame 2

Virtual address is converted to 0000000001001111101002 => 1001111101002 => 2048 + 256 + 128 + 64 + 32 + 16 + 4 = > **2548**

4.

a.) TLB hit, cache hit  
  
5ns (TLB access) + 12ns (cache access)  
  
b.) TLB miss, page table hit, cache hit  
   
 5ns (TLB access) + 25ns (page table reference) + 12ns (cache access)  
  
c.) TLB miss, page table hit, cache miss  
   
 5ns (TLB access) + 25ns (page table reference) + 12ns (cache access) + 25ns (main memory reference)  
  
d.) TLB miss, page table miss  
  
5ns (TLB access) + 25ns (page table reference) + 200ms (disk reference) + 5ns (TLB, since access is restarted) + 12ns (cache hit)

5.

a) 1/(1 - 0.9) + (0.9/2) = **1.81**

b) 1/(1 - 0.2) + (0.2/9) = **1.21**

6.

a) 8 surfaces x 1200 tracks per surface x 512 sectors per track x 512 bytes/sector

=> 2516582400 / 220

=> **2400MB**

b) Access time = [(60 seconds / 5400rpm) x (1000ms/seconds)] / 2

=> 5.555 + 4.5

=> **10.05 ms**